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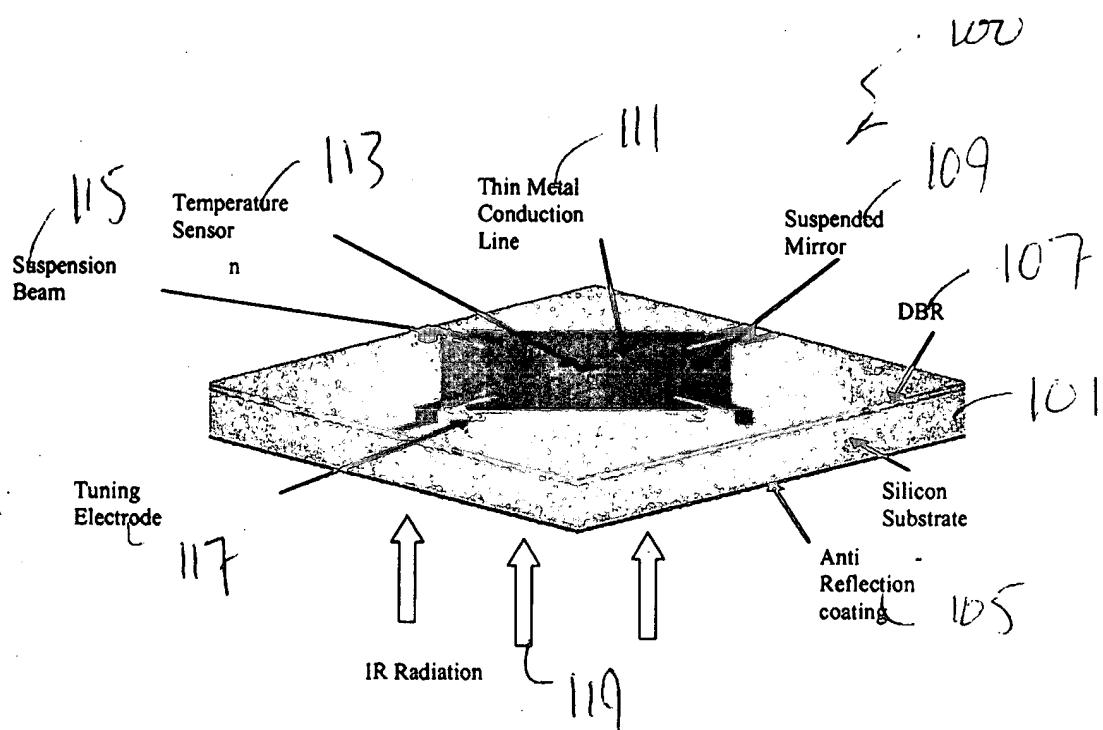


FIGURE 1

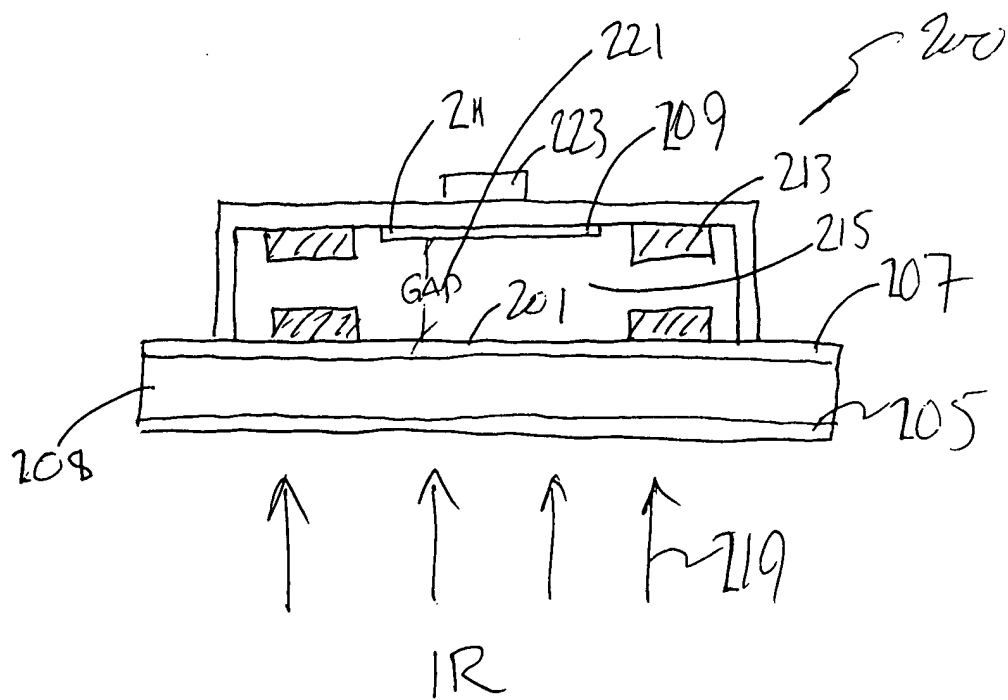


FIGURE 2

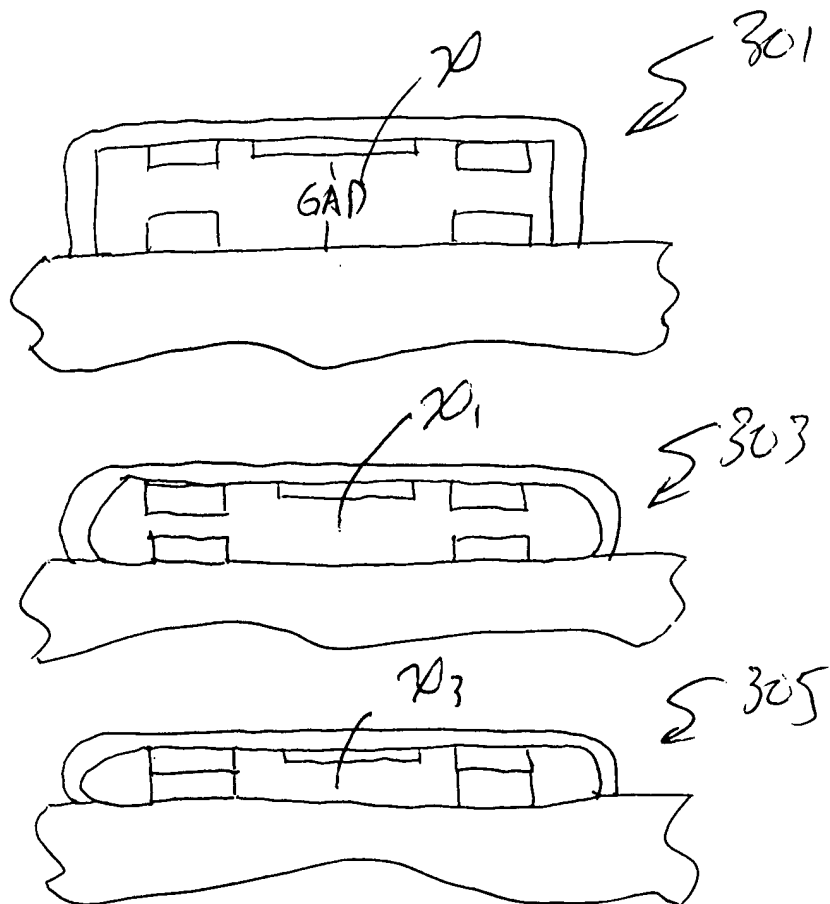


FIGURE 3

401 5 400



1: Deposit DBR Layers

FIG. 4



2: Deposit bottom electrode, Sputter Silicon, Deposit top mirror

FIG. 5



3: Deposit parylene and sensing film (e.g. VOx)

FIG. 6



4: Deposit Thin metal and Release Mirror in BrF3

FIGURE 7



Silicon Substrate



Low n material for DBR



Evaporated Bottom Metal Electrode



Sacrificial Layer (Amorphous Si or Photoresist + Amorphous Si)



Top Metal Electrode (Evaporated or Sputtered)



Parylene



Temperature Sensing Element (VOx or Ion-Implanted Parylene)



Evaporated Thin Metal (e.g. Titanium)

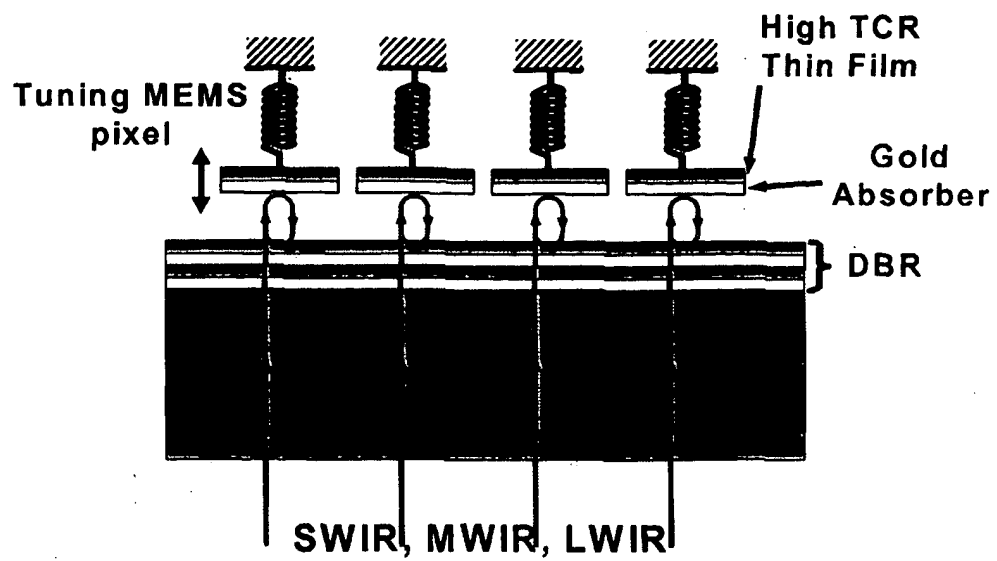
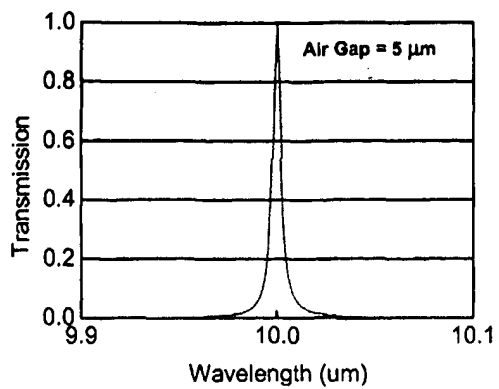
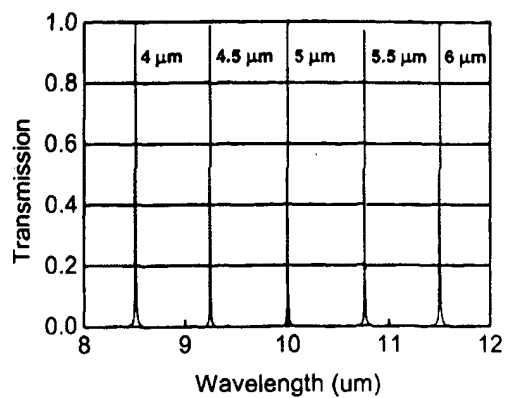


FIGURE 8



(a)



(b)

FIGURE 9

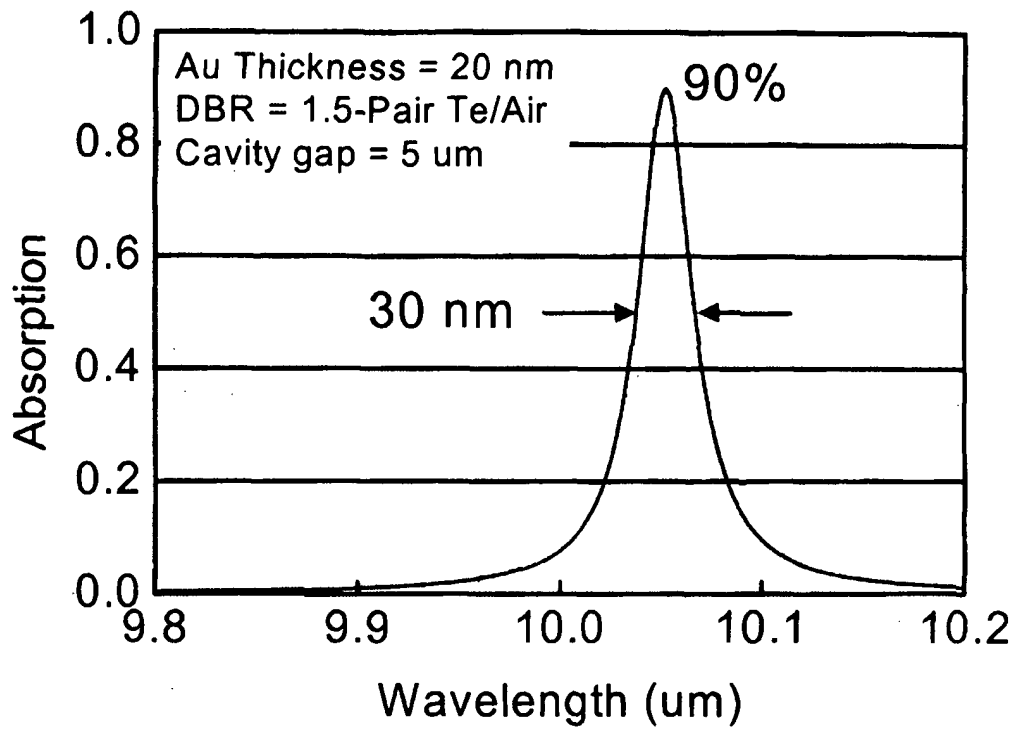


FIGURE 10

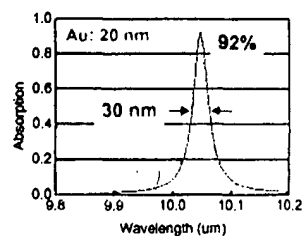
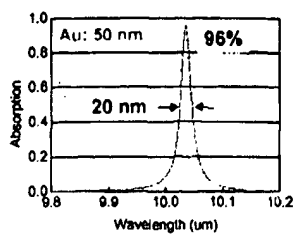
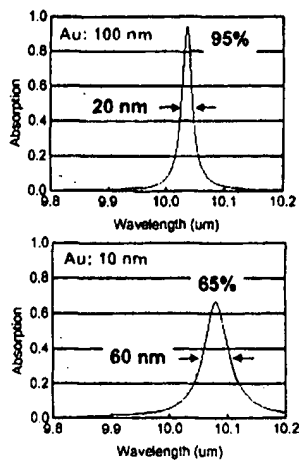


FIGURE 11

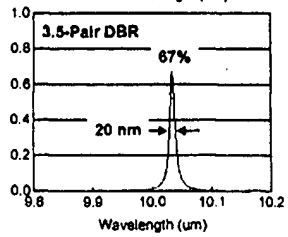
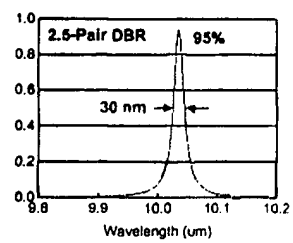
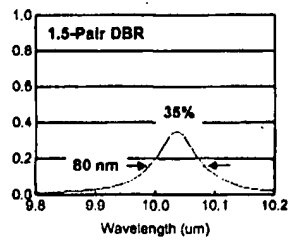
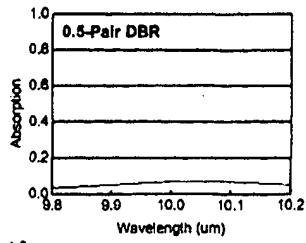


FIGURE 12

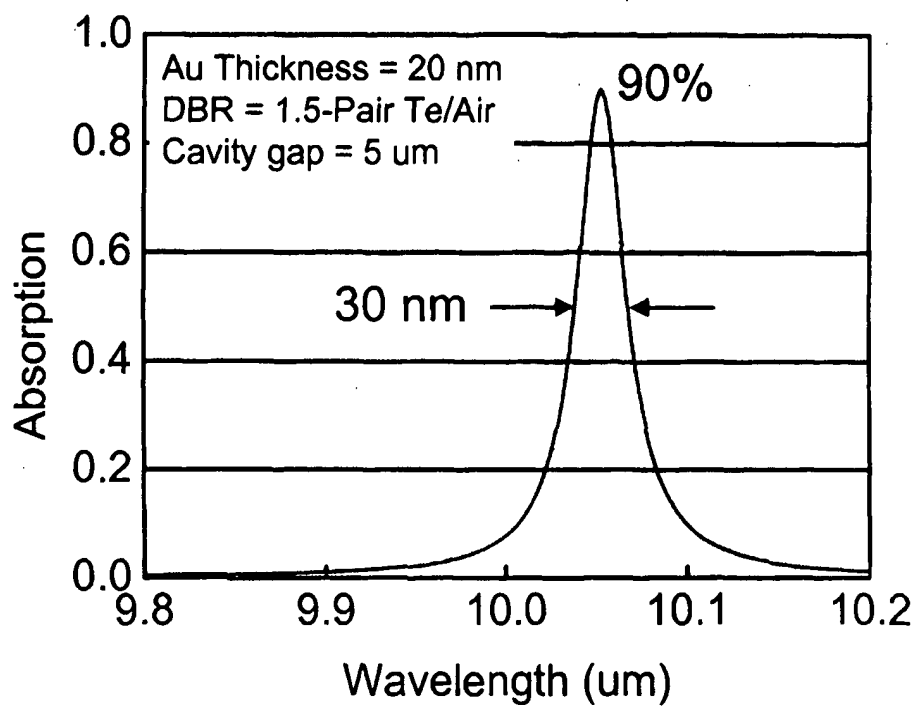


FIGURE 13

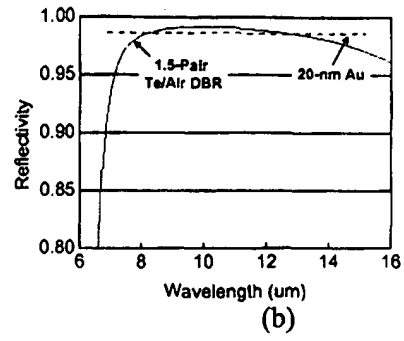
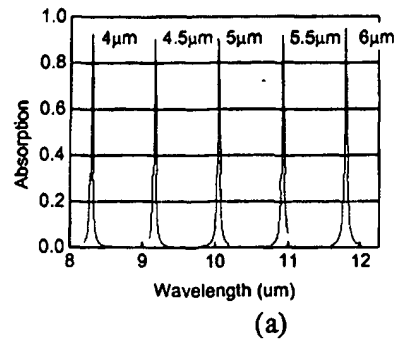


FIGURE 14